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# $\mathbf{CATC}^{^{\mathrm{TM}}} \mathbf{HPT}^{^{\mathrm{TM}}}$

# **USB Host Production Tester**

# **User's Manual**

#### Version 2.27

15 September 1999

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# 1. INTRODUCTION

The CATC HPT USB Host Production Tester is designed for use on the production line to test the Universal Serial Bus ports of USB-capable motherboards and PCs, according to the USB specifications. The HPT supports USB host implementations of both the Intel UHCI and Open HCI specifications.

CATC HPT Features:

- Intel 8x930 USB controller-based circuitry, packaged in a sturdy metal box
- DOS-based software program verifies functionality of the USB system under test
- supports UHCI and OHCI USB host implementations
- two cables enable simultaneous testing of two USB root ports in under 10 seconds
- tests for full- and low-speed port operation
- enclosure-mounted LEDs for second-level visual status and test verification
- can be incorporated into customer system test platforms (custom integration service available)
- tested for compliance with the USB specification
- one year warranty and hot-line customer support

The HPT box connects to the two USB ports of the USB Host PC unit under test, using two USB cables. The tester is an intelligent USB device, allowing for quick and accurate testing for proper USB device enumeration, data transfers, and detection of connection status for full- and low-speed devices, as well as the proper operation of USB host interrupt circuitry and the various USB status flags.

The HPT software program connects with the tester via the USB host controller on the motherboard. For each port, the HPT software checks for proper operation in both full- and low-speed modes. When all tests are successful, the software declares the USB host unit functional. Any failures are both displayed on the screen and saved as a text file. For units that fail these tests, a CATC Inspector<sup>™</sup> or Detective<sup>™</sup> USB Bus & Protocol Analyzer can be used to assist in debug and rework.

#### 1.1 USB Overview

USB is an open industry standard, providing a simple and inexpensive way to connect up to 127 devices to a single computer port. Keyboards, mice, tablets, digitizers, scanners, bar-code readers, modems, printers, and more can all run at the same time. USB devices plug into any platform that supports the standard, from notebooks to desktop PCs to workstations.

USB is a dynamically reconfigurable serial bus with an elementary data rate of 12,000,000 bits/sec, based on off the shelf, low cost micro-controller technology. Its modular layered software protocol supports sophisticated device drivers and application programs.

Please refer to the USB Specifications for details on the USB protocol. The USB specifications are available from the USB Implementers Forum at:

USB IF		
M/S JF2-51	Tel:	+1/ 503 264 0590
2111 NE 25th Avenue	Fax:	+1/ 503 693 7975
Hillsboro, OR 97124	Web:	http://www.usb.org/

#### 2. CATC HPT SYSTEM

The CATC HPT package includes the following components:

- a sturdy metal box housing the HPT electronic test circuitry, based on the Intel 8x930 USB controller
- an AC to DC converter
- two USB cables
- a diskette with the CATC HPT DOS software program
- this user's manual

The HPT box is an intelligent USB device. It has two female B-type USB connectors and two LEDs on the front of the unit and a +9V DC @ 500mA power connector on the rear. The USB connectors (marked "CH 1" and "CH 2") are used to connect the HPT box to the host under test. The power connector is used to power the box from the AC to DC power converter; when power is applied, the red LED (marked "PWR") is illuminated. The green LED (marked "STATUS") is a status indicator; it blinks to indicate that the on-board microcontroller is functioning properly.

The DOS-based HPT software runs on the USB host under test; it communicates with the HPT box via the USB host controller (on the motherboard). For each USB port, the software program checks for proper operation in both full- and low-speed modes. When all tests are successful, the software declares the USB host to be functional; any failures are reported on the computer display screen, and saved on the hard disk as a text file.

#### 3. SYSTEM SETUP

Position the CATC HPT box on the test bench, near the USB host to be evaluated.

Connect the DC plug of the AC to 9V DC @ 500mA power converter to the +9V power receptacle of the CATC HPT box. To activate the unit, plug the AC to DC converter into an appropriate AC power outlet.

In the USB test system, connect the USB HPT box as follows:

- A) Connect a USB cable between the USB connector labeled "CH 1" (on the CATC HPT box) and the USB port of the host system under test.
- B) If the system under test has a second USB port, use another USB cable to connect it to the USB connector labeled "CH 2" (on the CATC HPT box).

The CATC HPT USB Host Tester hardware is now ready for operation.

#### 3.1 Connectors and Cables

All connectors have a limited life (i.e., number of connect/disconnects before failure). When testing multiple hosts, be sure to **plug and unplug cables at the host only, not at the HPT box**. *There is generally no need to disconnect the B-type USB connectors from the HPT*. There is also no need to power down the HPT box between tests.

Additionally, forceful or otherwise improper connection and disconnection of USB cables can damage the cables and connectors on the USB host system and the CATC HPT box.

Note that the CATC Warranty (see "Warranty and License") specifically **excludes** damage caused by this kind of product misuse.

USB ports on the host PC under test can be connected to the HPT box in either order; this will only affect the sequence in which the ports are tested. The software will first test the port connected to "CH 1", then that connected to "CH 2".

Note: To observe bus traffic, a CATC Inspector or Detective USB Bus & Protocol Analyzer can be connected between the CATC HPT box and the host system under test.

# 4. SOFTWARE INSTALLATION

#### 4.1 Software Components

The CATC HPT software diskette includes the following files:

- USB\_HPT.EXE executable code of the CATC HPT program
- USB\_HPT.CFG configuration text file for the USB host controller (used only for Intel PIIX3 UHCI systems)

#### 4.2 Installing the software

Make a copy of the CATC diskette for backup, then copy **usb\_hpt.exe** (and also **usb\_hpt.cfg**, in the case of Intel PIIX3 UHCI systems) to the hard drive of the USB-capable host PC to be tested.

#### 4.3 Running the software

The HPT software program (**usb\_hpt.exe**) is a DOS application and must be run under the DOS operating system. It supports both UHCI and OHCI USB host controller implementations.

The program scans the PC's PCI devices and locates the USB host controller by class code. It uses the first host controller it finds as the test target. *On some systems with a USB-aware BIOS, the software may fail to communicate with the USB host controller; should this occur, contact CATC technical support (see "How to Contact CATC").* 

To run the program, type **USB\_HPT** at the DOS prompt and press the "Enter" key. The program will clear the monitor screen and begin execution. During the test, the program displays the test results on the monitor screen. The tests conclude in less than 10 seconds, leaving the test results on the screen. To terminate the program and get back to the DOS prompt, press any key.

#### 4.3.1 Setting the PIIX4 Interrupt Line Number

In some computers the BIOS does not set the PIIX4 interrupt line, and as a result, the USB host controller interrupt line remains disabled.

The HPT software allows setting of the PIIX4 interrupt line number, using the /I:N option, where N is the IRQ number of the USB host controller (in the range 3–F).

If the IRQ setting is done by the BIOS, the /I option is not required.

When thus directed, the HPT software reads the Interrupt Line Register contents (function 2). If a valid interrupt line number (3–F) is found, it uses this interrupt number *even if the /I option specifies a different IRQ number*. If an invalid interrupt value is found (not 3–F) the driver alerts the user with a screen message, stating that an invalid interrupt number was found, and requests the use of the /I option to specify a valid IRQ value.

Ignoring the /I option when a valid IRQ number is detected allows the user to use the same software configuration to run the HPT tester on different systems (where some need this option and some do not).

When the /I option is used, the driver writes the specified IRQ number to both the Interrupt Line Register and the PIRQD Route Control Register (function 0), and clears the Interrupt Routing Enable bit of the latter.

#### 4.3.2 Command Line Options

The test program supports a variety of command line options. To use these options, type **USB\_HPT** (at the DOS prompt) followed by one or more of the following options, and press the "Enter" key. Note that option switches may be either upper- or lowercase.

Options	Purpose	Default
/A[:TIME]	Specifies an integer value representing the number of milliseconds to wait at the end of the test before terminating (without waiting for the operator to press a key). The maximum value of "TIME" is 32,768 (approximately 32.8 seconds).	Wait for operator to press a key. Default value of "TIME" is 1000.
/B:Address	Valid for OHCI Host Controllers ONLY !!! Specifies (in HEX) the base address for the operational registers of the host controller	N/A
/C	Sends all screen output to the console (so it can be redirected to a file or communication port).	Display screen output only.
/D:DEVICE	Specifies (in HEX) a device ID for the host controller. Note: <i>In this case, the HPT software will not do automatic search</i> ; this option should be used in conjunction with option /V.	N/A

#### **Command Line Options**

/F:ON OFF	Turns the "create (test results) files" function on or off.	/F:ON (create files)
/I:n (n from 3–F)	Set PIIX4 interrupt line in USB host controller to specified IRQ number, unless already set by the BIOS (see "Setting the PIIX4 Interrupt Line Number", above).	Use IRQ as set by BIOS.
/P:X[,Y]	Specifies the (one or two) USB ports to be tested. If a single port is specified, it should be connected to the "CH 1" connector on the HPT box.	/P:1,2 (test ports 1 and 2)
/S:ON OFF	Turns the "end of test" indicator sound on or off.	/S:ON (sound on)
/V:VENDOR	Specifies (in HEX) a vendor ID for the host controller. Note: <i>In this case, the HPT software will not do automatic search</i> ; this option should be used in conjunction with option /D.	N/A
?	Displays this help information.	N/A

Examples:

1. USB_HPT /s:off /p:2	Test host USB port number 2 without activating the indicator sound.
2. USB_HPT /a /c > test.res	Terminate automatically one second after the test, and send the output to a file named "test.res".
3. USB_HPT /v:1042 /d:c068	Test a host controller with the specified vendor and device IDs.

# 5. HPT SOFTWARE FUNCTIONALITY

- The DOS-based HPT software runs on the USB host unit under test; it communicates with the HPT box via the USB host controller on the motherboard. For each USB port, the software program checks for proper operation in both full- and low-speed modes. When all tests are successful, the software declares the USB host to be functional; any failures are reported on the computer display screen, and saved on the hard disk as a text file.
- Initially, the test program attempts to determine (using the PCI protocol) whether or not the system under test is equipped with a USB Host Controller; if such a controller is not found, the program aborts with an explanatory error message.

# 5.1 Host Test Initialization

Once a USB host controller is identified, the HPT application proceeds to:

- 1. send a command to reset the USB Host Controller;
- 2. find the HPT test device connected to the USB port(s) under test (If not found, the program alerts the user—there may be a setup problem—and fails the test.);

- 3. reset the HPT test device to put it in a default condition;
- 4. enable the first USB port for communication with the HPT device; and
- 5. send a sequence of USB messages (as described below) to the HPT test device.

The application then issues commands to the HPT test device to execute a series of four (or two, if only one port is being tested) Port Test Sequences. If two ports are connected, the tests are performed in the following order:

full-speed test sequence at the port connected to "CH 1"

low-speed test sequence at the port connected to "CH 1"

full-speed test sequence at the port connected to "CH 2"

low-speed test sequence at the port connected to "CH 2"

Prior to conducting each test sequence, the program checks for the correct Connection Status and Connection Change Status for both USB ports.

# 5.2 Port Test Sequence

As a principal element of the host production test, the CATC HPT software sends a specific USB message sequence to the HPT test device. For each test sequence the following items are verified:

- data returned properly by the device (successful IN/OUT transfers);
- correct status for each transfer;
- proper USB Interrupt functionality (interrupt on completion for each transfer); and
- absence of host controller process errors, host system errors, and USB protocol errors

The test sequence includes the USB messages enumerated below. The specific USB packets involved are illustrated using data captured on the bus by a CATC Detective USB Bus & Protocol Analyzer during actual HPT tests.

#### 5.2.1 Set Address

The first control transfer issued by the HPT application program sets the HPT test device address to 1. All subsequent USB transfers use this address.

Packet#	Sync	SETUP	ADDR	ENDP	CRC5	Idle		
2	00000001	0×B4	0×00	0×0	0×08	3		
	_							
Packet#	Sync	DATAO		D	АТА		CRC16	Idle
3	00000001	0xC3	00	05 01 0	0 00 00 0	0 00	0xD7A4	3
				_				
Packet#	Sync	ACK	Idle					
4	00000001	0×4B	11801					

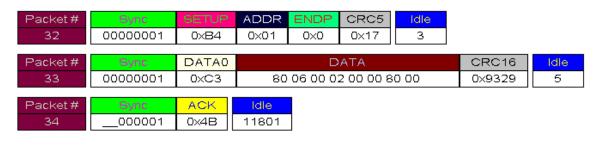
# 5.2.2 Get Device Descriptor

The application program then sends a standard device request ("GET\_DESCRIPTOR") message. The HPT test device returns its 18-byte device descriptor, using multiple IN transactions in the data stage.

	Packet#	Sync	SETUP	ADDR	ENDP	CRC5	Idle		
	12	00000001	0×B4	0×01	0×0	0×17	3		
	Packet#	Sync	DATAO		D	ATA		CRC16	Idle
	13	00000001	0xC3	80	06 00 0	1 00 00 8	0 00	0xB129	4
	Packet# 14	Sync 00000001	ACK 0x4B	<mark>ldle</mark> 11800					
•••									
	Packet# 17	Sync 00000001 (	IN ADDF )x96 0x01	R ENDP	CRC5 0x17	ldle 4			
	Packet# 18		DATA1 DXD2	12 01	1 00 01 FF		TA 23 04 34 12	01 00 00 00	
	Packet# 19	· · · · ·	A <mark>CK Idle</mark> )x4B 1173						

#### 5.2.3 Get Configuration Descriptor

The application program next sends a standard device request ("GET\_CONFIGURATION") message. The HPT test device returns its 39-byte configuration descriptor, using multiple IN transactions in the data stage.

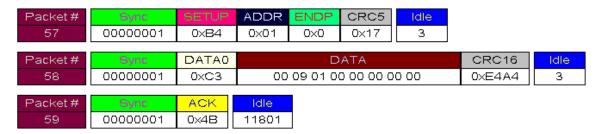


•••

Packet#	Sync	IN	ADDR	ENDP	CRC5	Idle
37	00000001	0×96	0×01	0×0	0×17	5
	-					
Packet#	Sync	DATA1				DATA
38	_0000001	0xD2		09 02	27 00 0°	1 01 00 40 18 09 04 00 00 03 FF FF (
						· · · · · · · · · · · · · · · · · · ·
Packet#	Sync	ACK	Idle			
39	00000001	0×4B	11730			

# 5.2.4 Set Configuration

The application program sends another standard device request ("SET\_CONFIGURATION") message. After receiving this request, the HPT test device sets its current configuration to 1, enables bulk transfer endpoints 1, 2, 3, and stands by to send and receive through bulk transfers.



#### 5.2.5 Bulk Read

The HPT test device now sends a 64-byte IN packet through endpoint 1: data 0x00 through 0x3E, plus a final byte that reflects the power status of the two USB ports on the test device (see "USB Power State Test" below for discussion of power status). This step is performed twice (i.e., two 64-byte transfers).

Last Byte	Port 1 Power Status	Port 2 Power Status
0x3F	Good	Good
0xF0	Bad	Good
0x0F	Good	Bad
0x00	Bad	Bad

Packet#	Sync	IN	ADDR	ENDP	CRC5	Idle					
67	00000001	0×96	0×01	0×1	0×1A	4					
Packet# 68	Sync 00000001	DATA0 0×C3									
							DATA				
	00 01 02 03	3 04 05 0	6 07 08	09 0A 0E	3 OC OD	0E 0F 10	) 11 12 13	14 15	16 17 18	3 19 1A	1B 1C 1
	24 25 26 27	7 28 29 2	A 2B 2C	2D 2E 2	2F 30 31	32 33 34	1 35 36 37	38 39 3	3A 3B 3	C 3D 38	EOF
	CRC16 0x64C7	Idle 6									

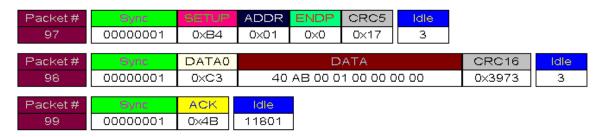
#### 5.2.6 Loopback Test

The HPT test device is programmed to send back to the host, through endpoint 2, the same data it receives from the host through endpoint 3. In the loopback test, the USB HPT program sends a 16-byte OUT packet through endpoint 3 followed by a 16-byte bulk read (to read the data back from endpoint 2). This step is also performed twice (i.e., four 16-byte transfers; two OUT and two IN). The program checks that all data received correspond to the data sent.

Packet#	Sync	OUT ADD	R ENDP CRC5 Idle
77	00000001	0×87 0×01	1 0x3 0x0E 3
Packet#	Sync	DATAO	DATA
78	00000001	0×C3	00 00 31 32 33 34 35 36 37 38 39 3A 3B 3C 3D 3E (
Packet#	Sync	ACK Idl	le l
79	000001	0×4B 117	736
Packet#	Sync	SOF Fran	
80	00000001	0×A5 0×0	020 0×19 11962
Destudet			
Packet#	Sync		me # CRC5 Idle
81	00000001	0×A5 0×0	021 0x06 5
Packet#	Sync	IN ADD	R ENDP CRC5 Idle
82	00000001	0×96 0×01	1 0×2 0×03 5
Packet#	Sync	DATAO	DATA
		0.00000000000	
83	_0000001	0×C3	00 00 31 32 33 34 35 36 37 38 39 3A 3B 3C 3D 3E (
Packet#	Sync	ACK Idl	le
84	00000001	0×4B 117	

#### 5.2.7 Connection/Disconnection Ability

The application program sends a device specific request to allow the HPT test device to disconnect itself from the bus and to reconnect after a short period as either a full- or low-speed device. The HPT program checks the port status registers to ensure that both disconnect and connect events concluded properly.



#### 5.3 USB Power State Test

The HPT test device checks that the USB host is supplying 5V DC power on the USB bus, between the power and ground pins of the USB connectors. (The test device does not measure the amount of DC current supplied by the USB host.) During each port test sequence, the HPT test device sends power state information for both USB ports to the host. The application collects and compares this information, and displays it at the end of the test. If all (two or four) functional test sequences fail, the application displays "N/A" for the power state.

#### 5.4 Test Results: Monitor Display

Results of the tests are displayed on the computer monitor screen. If all test functions succeed, the overall test is declared "passed"; otherwise, it is reported as "failed".

Following is a typical HPT displayed result for a passed test (in which USB Port 1 is connected to "CH 1"):

Found USB HC, VENDOR ID	= XXXX
Full Speed at Port 1 :	PASSED
Connection status :	OK
Error count :	0,0,0,0
USB interrupt count :	OK
Low Speed at Port 1 :	PASSED
Connection status :	OK
Error count :	0,0,0,0
USB interrupt count :	OK
Full Speed at Port 2 :	PASSED
Connection status :	OK
Error count :	0,0,0,0
USB interrupt count :	OK
Low Speed at Port 2 :	PASSED
Connection status :	OK
Error count :	0,0,0,0
USB interrupt count :	OK
POWER: Port1 - GOOD; Port2	- GOOD
TEST PASSE	D

For failed tests, the results may differ as follows:

- PASSED will be changed to FAILED if data received on the data loopback test doesn't match the expected data, or to NO DEVICE if the test device was not found connected to the USB port at the beginning of the test sequence.
- Connection Status will be changed to BAD if the Connection Change bit wasn't set for both disconnect and connect events.
- Non-zero error counts can occur. Errors are grouped into four classes, and displayed in the following order:
  - 1) USB errors
  - 2) host system errors
  - 3) host controller process errors
  - 4) wrong transfer status errors
- For example, an error count of "2,0,1,0" is interpreted to mean that there have been two "USB errors", no "host system errors", one "host controller process error", and no "wrong transfer status errors". See below for an interpretation of these errors.

- If the USB interrupt count doesn't match the expected count (21), it will be displayed as WRONG, followed by a number representing the actual USB interrupts encountered.
- The power state will be displayed as BAD if power wasn't provided by the host on the corresponding USB port. If *all* test sequences failed for a particular USB port, the power state is displayed as N/A.

HPT Error Class:	UHCI Error Type:
USB errors	The Host Controller sets this bit when completion of a USB transaction results in an error condition (e.g., error counter underflow). If the Transfer Descriptor on which the error interrupt occurred also had its IOC bit set, both this bit and Bit 0 are set.
host system errors	The Host Controller sets this bit when a serious error occurs during a host system access involving the Host Controller module. In a PCI system, such errors include PCI Parity error, PCI Master Abort, and PCI Target Abort. When this error occurs, the Host Controller clears the Run/Stop bit in the Command register to prevent further execution of scheduled Transfer Descriptors.
host controller process errors	The Host Controller sets this bit when it detects a fatal error; it indicates that the Host Controller suffered a consistency check failure while processing a Transfer Descriptor. An example is finding an illegal PID field while processing the packet header portion of the Transfer Descriptor. When this error occurs, the Host Controller clears the Run/Stop bit in the Command register to prevent further execution of scheduled Transfer Descriptors.
wrong transfer status errors	This bit is set when one of the error bits (i.e., Stalled, Data Buffer Error, Babble Detected, or CRC/Time Out Error) in the status field of a transfer is set upon completion.

For UHCI systems, the HPR error classes are interpreted as follows:

Note: If, at the beginning of a test, the HPT software senses that the HPT device is not connected to either one of the USB ports, the program declares a test failure, displaying the message:

Found USB HC, VENDOR ID = XXXX

Test device improperly connected to the USB port(s) under test!

TEST FAILED

# 5.4.1 OHCI Error Reporting

The above HPT error messages are used for OHCI systems as well. However, the specific HPT error classes are interpreted differently for OHCI, as follows:

HPT Error Class:	OHCI Error Type:
USB errors	Data Toggle Mismatch, Stall, Device Not Responding, PID Check Failure, Unexpected PID, Data Overrun/Underrun, Buffer Overrun/Underrun, or Not Accessed error (completion codes)
host system errors	Unrecoverable Error (status register UE)
host controller process errors	Scheduling Overrun (status register SO)
wrong transfer status errors	CRC or Bit Stuffing error (completion codes)

#### 5.5 Test Results: Disk Files

The HPT application generates two text files (unless disabled with the /F:OFF switch): one with the extension "**.sta**", another with the extension "**.fal**". The root name of both files is constructed from the current date, as "month\_day\_year". For example, on 3 July 1997 the file names will be:

#### 7\_3\_97.sta and 8\_3\_97.fal

In the ".sta" file, the program records production statistics for the current day: the number of units passed and the number of units failed.

In the ".fal" file is recorded a failure description for each failed unit, as follows:

Failure #n, Unit #m

followed by one of:

The USB Host Controller wasn't found in the system.

The TEST DEVICE wasn't connected to USB ports.

Started at port *n*. First failure for Full (Low) Speed at port *m*. Type of failure:

the latter followed by one or more of:

Wrong data on data loopback.

Bad connection status.

There were *v* USB errors.

There were *w* host system errors.

There were *x* host controller process errors.

There were *y* wrong transfer status errors.

The number of USB interrupts was wrong: *z* instead of 21.

USB power is not provided on port 1.

USB power is not provided on port 2.

#### **5.6 Test Results: Error Levels**

Upon termination, the HPT application sets the DOS error level according to the test results. If the test passed, it exits with error level 0; otherwise, it exits with a corresponding error level. This feature allows processing of the test results in a batch file.

The error level is calculated according to the following rules:

(1) To identify where the failure occurred, an error base value is selected from the following table:

"CH 1" connected to:	Error occurred at test of:	Error Base Value:
Host Port 1	Full Speed At Port 1	1
Host Port 1	Low Speed At Port 1	5
Host Port 1	Full Speed At Port 2	9
Host Port 1	Low Speed At Port 2	13
Host Port 2	Full Speed At Port 2	17
Host Port 2	Low Speed At Port 2	21
Host Port 2	Full Speed At Port 1	25
Host Port 2	Low Speed At Port 1	29

(2) To identify the specific error, one of the following four values is added to the base:

Added to base value:	Reason:
0	incorrect data during enumeration or data loopback tests
1	correct data, but bad connection status
2	data & connection good, but a non-zero error count
3	above tests passed, but incorrect USB interrupt count

If, for example, the program terminated with error level 30 (base value = 29, +1), it means:

- "CH 1" was connected to Host Port 2, thus testing began with Port 2.
- Port 2 was tested at both full- and low-speed, and data was good.
- Port 1 was good at full speed.
- There was bad connection status for low speed at port 1.

If the program terminated with error level 4 (base value = 1, + 3), it means:

- "CH 1" was connected to Host Port 1, thus testing began with Port 1.
- Port 1 was tested at full-speed and the data came through as expected.
- The controller couldn't interrupt the host

If all the functional tests pass, but the power status is bad, the error levels will be:

Error level:	Reason:
33	no power on port 1
34	no power on port 2
35	no power on port 1 or port 2

Finally, if—at the beginning of the test—the HPT software does not find an HPT test device connected, the program returns error level 36. If no USB host controller is detected, error 37 is returned.

Error level:	Reason:	
36	no port connected	
37	no USB host found	

# 5.7 Configuration File Information

# 5.7.1 For Intel PIIX3 UHCI systems only

If the system under test has a BIOS that disables the USB portion of the Intel PIIX3 Host Controller, the HPT software will enable it for the duration of the test, and then restore the previous settings.

In order to run the test, the software needs certain information about the controller configuration: the I/O base address for PIIX3 function 2 (USB portion), the IRQ assigned to the host controller, and the USB Clock Selector (if host controller runs at 24 or 48 MHz).

In order to provide this input, a configuration text file (**usb\_hpt.cfg**) is included with the HPT software, containing two lines, as in the following example:

; I/O Space	IRQ	Clock
0xF300	11	48

This file should be used to provide input for the above cases. If the ".cfg" file is not present, the program will use the default values as shown above (0xF300 11 48). For the clock input, only two values are accepted: 24 and 48; any other values are ignored, and 48 used as a default. The I/O base address should be entered in hexadecimal, IRQ as an integer.

The values in **usb\_hpt.cfg** are used by the program only when the USB (Function 2 in PIIX3) is disabled by the BIOS.

# 5.7.2 For Systems Running EMM386

Systems with an OHCI host controller that are utilizing EMM386, MUST specify the following "RAM" option in their EMM386.exe statement:

```
Device=emm386.exe RAM X=d0000-d1000
```

For systems utilizing the UHCI host controller, the RAM option is not required.

# 6. HOW TO CONTACT CATC

Type of Service	Contact
Call for technical support	US and Canada: +1/ 800 909 2282
	Worldwide: +1/ 408 727 6600
Fax your questions	Worldwide: +1/ 408 727 6622
Write a letter	Computer Access Technology Corp. Customer Support 2403 Walsh Avenue Santa Clara, CA 95051-1302
Send e-mail	support@catc.com
Visit CATC's Website	http://www.catc.com/

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